In the claims:

1.An adder comprising:

a carry select adder and

a carry increment adder.

2. The adder of Claim 1 wherein said carry select adder is used for the most significant bits.

3. The adder of Claim 1 wherein said adder comprises multiple blocks and wherein said carry select adder is used in a block for the most significant bits ; said carry increment adder is used in the block for the least significant bits and a mixed carry increment adder and carry lookahead adder circuit are used in a middle bit block.

4. The adder of Claim 1 including multiple carry increment adders with at least one of said carry increment adders used with a carry lookahead adder.

5. The adder of Claim 4 wherein all of said carry increment adders are used with a carry lookahead adder.

6. A multiple block adder comprising:

a carry select adder block including most significant bit or sign bit; and

a carry increment adder block.

7. A multiple block adder comprising:

a carry select adder block for the most significant bits; and

a carry increment adder block for less significant bits.

8.The adder of Claim 4 wherein said carry increment adder block is used with carry lookahead circuit for a least one of the less significant bit blocks.